AMENDMENTS TO THE CLAIMS

Claims 1-7. (Cancelled)

8. (Currently Amended) A method of representing resources of ~~a plurality of programmable hardware tiles included in~~ a programmable logic device (PLD), ~~each hardware tile including common routing resources common to all of the hardware tiles and unique logic resources unique to each hardware tile~~, the method comprising:

generating a plurality of instances of a common software tile from a first source code definition of the common software tile comprising a description of [[the]] common routing resources, ~~the common software tile having~~ of first terminals for coupling an instance of the common software tile to other instances of the common software tile, and ~~further having~~ of second terminals; and

generating~~, for each hardware tile,~~ a plurality of instances of each of a plurality of [[a]] unique software tiles from respective source code definitions of the plurality of unique software tiles, each respective source code definition comprising a description of [[the]] unique logic resources ~~included in the hardware tile~~, ~~each unique software tile comprising~~ and of terminals for coupling an instance of the unique software tile to the second terminals of an instance of the common software tile, wherein the first source code definition of the common software tile and the respective source code definitions of the unique software tiles are separate data structure definitions.

9. (Currently Amended) The method of Claim 8, wherein:

each respective source code definition of a unique software ~~hardware~~ tile further includes unique routing resources unique to [[each]] the unique software ~~hardware~~ tile; and

generating an instance of the unique software tile ~~for each hardware tile further~~ comprises generating a unique description of the unique routing resources included in the unique software ~~hardware~~ tile.

10. (Original) The method of Claim 8, wherein the PLD is a Field Programmable Gate Array (FPGA).

11. (Currently Amended) The method of Claim 10, wherein the unique logic resources comprise ~~plurality of programmable hardware tiles comprises~~ at least one of the following types of logic blocks: configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks.

12. (Currently Amended) The method of Claim 11, wherein the unique logic resources comprise ~~plurality of programmable hardware tiles further comprises~~ input/output blocks (IOBs).

13. (Currently Amended) The method of Claim 8, further comprising generating a PLD device model representing a placement of the ~~plurality of programmable hardware tiles in the PLD and comprising~~ instances of the common software tile and the unique software tiles~~, the PLD device model~~ utilizing a uniform numbering scheme based on numbered instances of the common software tile.

14. (Currently amended) The method of Claim 8, wherein the plurality of ~~programmable hardware~~ instances of the common software tile and the unique software tiles comprise ~~comprises~~ an entirety of the programmable hardware tiles in the PLD.

Claims 15-21. (Cancelled)

22. (New) An article of manufacture, comprising:

a processor-readable program storage medium configured with processor-executable instructions for representing resources of a programmable logic device (PLD), by performing the steps including,

generating a plurality of instances of a common software tile from a first source code definition of the common software tile comprising a description of common routing resources, of first terminals for coupling an instance of the common software tile to other instances of the common software tile, and of second terminals; and

generating a plurality of instances of a plurality of unique software tiles from a respective source code definitions of the plurality of unique software tiles, each respective source definition comprising a description of unique logic resources, and of terminals for coupling an instance of the unique software tile to the second terminals of an instance of the common software tile, wherein the first source code definition of the common software tile and the respective source code definition of the unique software tile are separate data structure definitions.

23. (New) The article of manufacture of Claim 22, wherein:

each respective source code definition of a unique software tile further includes unique routing resources unique to the unique software tile; and

generating an instance of the unique software tile comprises generating a unique description of the unique routing resources included in the unique software tile.

24. (New) The article of manufacture of Claim 22, wherein the PLD is a Field Programmable Gate Array (FPGA).

25. (New) The article of manufacture of Claim 24, wherein the unique logic resources comprise at least one of the following types of logic blocks: configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks.

26. (New) The article of manufacture of Claim 25, wherein the unique logic resources comprise input/output blocks (IOBs).

27. (New) The article of manufacture of Claim 22, further comprising generating a PLD device model representing a placement of the instances of the common software tile and the unique software tiles utilizing a uniform numbering scheme based on numbered instances of the common software tile.

28. (New) The article of manufacture of Claim 22, wherein the plurality of instances of the common software tile and the unique software tiles comprise an entirety of the programmable hardware tiles in the PLD.

29. (New) A processor-based method for representing resources of a field programmable gate array (FPGA), comprising:

establishing in a computer memory, a plurality of instances of a first type tile from a source code specification of the first type tile, wherein the source code specification of the first type tile specifies a programmable switch matrix, a first set of pins for coupling to instances of the first type tile, and a second set of pins; and

establishing in a computer memory from respective source code specifications of a plurality of unique types of tiles, a respective plurality of instances for each of the plurality of unique types of tiles;

wherein each source code specification of a unique type tile specifies a set of logic resources that is different from sets of logic resources of all others of the plurality of unique types of tiles and a set of pins for coupling an instance of the unique type tile to an instance of the first type of tile, and the source code specifications of the plurality of unique types of tiles and of the first type of tile are separate data structure definitions.

30. (New) The method of Claim 29, wherein the sets of logic resources of the unique types of tiles include configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks.

31. (New) The method of Claim 30, wherein the sets of logic resources of the unique types of tiles further include input/output blocks (IOBs).

32. (New) The method of Claim 29, further comprising representing in a computer memory relative placement of the instances of the first type tiles and instances of the unique type tiles based on row and column designations of the instances of the first type tiles.